IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

In re Patent Application of Atty Dkt. 124-812
C# M#

JEFFERSON et al. Group Art Unit: 2826

Serial No. 09/701,884 Examiner: Kevin Quinto

Filed: December 5, 2000 Date: October 30, 2003

Title: QUANTUM WIRE FIELD-EFFECT TRANSISTOR AND METHOD OF MAKING THE SAME

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By Atty: Stanley C. Spooner, Reg. No. 27,393

Signature: _____

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

JEFFERSON et al

Atty. Ref.: **124-812**

Serial No. **09/701,884**

Group: **2826**

Filed: **December 11, 2000**

Examiner: **K. Quinto**

For: **QUANTUM WIRE FIELD-EFFECT TRANSISTOR AND METHOD OF MAKING THE SAME**

* *

APPEAL BRIEF

On Appeal From Group Art Unit 2826

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I. REAL PARTY IN INTEREST

The real party in interest in the above-identified appeal is QinetiQ Limited by virtue of an Assignment from the inventors to The Secretary of State for Defence recorded April 19, 200, at Reel 11723, Frame 429, and a subsequent Assignment from The Secretary of State for Defence to QinetiQ Limited recorded February 20, 2002, at Reel 012831, Frame 459.

II. RELATED APPEALS AND INTERFERENCES

There are believed to be no related appeals or interferences with respect to the present application and appeal.

III. STATUS OF CLAIMS

Claims 1-32 are pending in the application, with the Examiner contending that claims 1-7, 9, 10, 12-21, 23-26, 29, 30 and 32 are rejected and claims 8, 11, 22, 27, 28 and 31 are objected to.

IV. STATUS OF AMENDMENTS

No amendments have been submitted with respect to the second non-final Official Action mailed March 31, 2003.

V. SUMMARY OF THE INVENTION

The present invention generally relates to an improved structure for a transistor and methods for creating such an improved transistor.

In particular, the present invention relates to single electron transistors (SET) which utilizes two semiconductor compounds of different band gaps where the charge carriers are confined to a potential or quantum well. In such devices, if the charge carriers are electrons, a two-dimensional electron gas is formed, and if the charge carriers are holes, then a two-dimensional hole gas is formed.

In the SET, the electron (or hole) gas is further confined by external gates so as to form a so-called quantum dot which is of such a size that it can hold only a few electrons, typically between zero and twenty. Such devices operate because the quantum dot has small capacitance and the energy required to move electrons is quite large. If the device is cooled to very low temperatures, the electron thermal energy becomes less than the charging energy. The capacitance of the quantum dot is so small that the addition of a single electron to the potential well significantly increases the electrostatic energy. Without a significant source-drain voltage bias, the electrons cannot travel through the quantum dot.

In the past, such devices are traditionally confined to operate at relatively low temperatures, typically less than liquid nitrogen temperatures. As would be apparent, it often is inconvenient to carry around liquid nitrogen so as to cool SET devices for their operation. Thus, it is an ongoing aim to increase the operating temperature of such devices. Prior art attempts to do so require precise patterning and etching of structures to provide further confinement of the two-dimensional

electron gas. However, the necessary reduction in size in order to obtain higher operating temperature quantum devices is not possible with conventional lithography and etching. Standard optical lithography permits feature sites of 0.1 microns and a registration of substantially ± 0.3 microns. Even using electron beam lithography, the feature size is only decreased to 30 nm with a registration of 100 nm.

Appellants have found that an SET can be provided by creating a substantially one-dimensional elongate conductor (14 in Fig. 2) in a groove (6 in Fig. 2) and locating the groove in a second semiconductor (12,13 in Fig 2), where in a preferred embodiment the second semiconductor is actually two layers (12,13) with the substantially one-dimensional elongate conductor (14) located therebetween. This substantially one-dimensional elongate conductor extends between source and drain electrodes (24, 26) and includes at least one further electrode acting as a gate electrode (16, 18 in Figs. 1 and 2).

The fact that the substantially one-dimensional elongate conducting means is located in the groove within the second semiconductor ensures it is sufficiently small to be substantially one-dimensional. Additionally, the groove is oriented such that at least one wall of the groove is substantially parallel to a crystal plane on which the first semiconductor is substantially zero. This substantially zero growth rate ensures that the substantially one-dimensional elongate conducting

means does not expand during growth in any other directions and therefore retains its "substantially one-dimensional" characteristics.

The one-dimensional elongate conductor, because it is small enough in all directions except for its "one-dimensional" direction, can be thought of as a quantum wire which operates with one-dimensional conduction. While v shaped groove quantum wires are well known, especially in the field of basic physics and application to optical devices, it is not known to connect such a structure between source and drain electrodes and provide a further electrode acting as a gate electrode in the region of the one-dimensional elongate conductor.

Thus, the present invention is characterized by the creation of a single electron transistor (SET) comprising at least one "**substantially one-dimensional, elongate conducting means**" which is embodied by "**a first semiconductor substantially surrounded by a second semiconductor**" and "**extending between source and drain electrodes.**" A "**further electrode in the region of the one-dimensional elongate**" conductor is provided. The elongate conductor is provided "**in a groove within the second semiconductor**" with the groove oriented such that "**at least one wall of the groove is a, substantially planar, surface, substantially parallel to a crystal plane on which the growth rate of the first semiconductor is substantially zero.**"

VI. ISSUES

Whether claims 1-7, 9, 10, 12-21, 23-26, 29, 30 and 32 are obvious over the combination of Kizuki in view of Bestwick in further view of Chapple-Sokol and further in view of Doyle.

VII. GROUPING OF CLAIMS

The rejected claims stand or fall together based upon the patentability of independent claim 1.

VIII. ARGUMENT

1. Discussion of the References

Kizuki (U.S. Patent 5,679,962) is an example of a prior art single electron transistor (SET). Specifically, Kizuki teaches a number of quantum wires (shown as items 7 in Fig. 1) that are formed by soft confinement, i.e. there are electric fields applied by the saw-tooth structure labeled 4 to define an elongate conducting means. As shown in Kizuki Figure 9, gate 12, source 10 and drain 11 electrodes are disclosed.

However, Kizuki does not teach that the substantially one-dimensional elongate conductor is provided by a first semiconductor substantially surrounded by a second semiconductor, nor does it disclose the locating of the elongate conductor within a groove, or in a groove where one wall has a substantially zero growth rate with respect to the first semiconductor material. As will be apparent to

those of ordinary skill in the art, the "soft confinement" of Kizuki is not the same as the hard confinement of the present invention, i.e. the location of the substantially one-dimensional elongate conductor within and surrounded by the second semiconductor, i.e. layers 12 and 13 in appellants' Figure 2. Instead, in Kizuki the quantum wire channel is generated by electric fields produced by the triangular cross-section structure, labeled 3 and 4 in the Kizuki reference. This soft confinement is not the same as appellants' hard confinement in which the substantially one-dimensional elongate conductor is substantially surrounded by a second semiconductor (layers 12 and 13) and located in the bottom of a groove.

Bestwick et al (U.S. Patent 5,571,376) does not describe a SET. Bestwick merely describes a v-groove quantum wire, i.e. a hard confined quantum wire. There is no suggestion that the hard confined quantum wire could be combined with source, drain or further electrodes in order to form a single electron transistor.

Chapple-Sokol et al (U.S. Patent 5,612,255) teaches the creation of quantum wire channels that have high electron mobility. This reference does not describe an SET and instead describes a standard field effect transistor (FET) which is formed from a quantum wire. There is no elongate conducting means formed from a first semiconductor material surrounded by a second semiconductor material, nor is there any disclosure of forming the elongate conducting means in a v-groove arrangement.

Doyle et al (U.S. Patent 6,063,688) also teaches an FET and not an SET. The structure of Doyle is similar to the structure in Chapple-Sokol, i.e. forming an FET from a quantum wire, and does not include any disclosure or teaching of an elongate conductor formed from a first semiconductor material surrounded by a second semiconductor material, nor does it teach the groove requirement in the present invention.

2. Discussion of the Rejection

Claims 1-7, 9, 10, 12-21, 23-26, 29, 30 and 32 stand rejected under 35 USC §103 as being unpatentable over Kizuki in view of Bestwick, further in view of Chapple-Sokol and further in view of Doyle. To the extent the rejection is understood, the Examiner appears to find claimed elements in the various references, although those references, with the exception of Kizuki, have nothing to do with a single electron transistor.

Kizuki teaches a conventional prior art single electron transducer which has no disclosure of the claimed construction method. The Examiner admits that the Bestwick reference "does not explicitly disclose the use of the quantum wire in a transistor structure." The Examiner cites the Chapple-Sokol and Doyle references, which as noted above are FETs (and not SETs), as disclosing quantum wire channels with high electron mobility for high-speed operation. The Examiner apparently believes that Kizuki, in teaching a prior art SET, renders obvious the

combination of elements taken from the Bestwick, Chapple-Sokol and Doyle references.

The Examiner, instead of providing a reason or motivation for combining elements from the various references, merely concludes that "it would be obvious to use the quantum wire of Bestwick as the channel of Kizuki so as to attain a device with high electron mobility."

3. The Errors in the Rejection

There are at least four significant errors in the second non-Final Rejection and they are summarized as follows:

(a) Only the Kizuki reference relates to a single electron transistor (SET);

(b) Kizuki teaches away from the claimed combination of elements;

(c) No cited reference suggests the problem solved by the present invention, i.e. SET operation at higher temperatures; and

(d) The Examiner fails to provide any reason or motivation for combining any of the prior art references.

Specifically, the Examiner is reminded that the Court of Appeals for the Federal Circuit has held that "the PTO has the burden under Section 103 to establish a *prima facie* case of obviousness." *In re Fine*, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

With respect to the combination of references, the Federal Circuit has also held that "teachings of references can be combined *only* if there is some suggestion or incentive to do so." *Id.* at 1599. Here the Examiner has provided no support for the allegation of it being obvious to combine these references.

The Federal Circuit has also opined that it is "error to find obviousness where references 'diverge from and teach away from the invention at hand'." *Id.* As noted above, the references all are believed to teach solutions to problems other than higher temperature operation and thus teach away from the claimed invention.

With respect to the alleged motivation for combining these references, the Examiner has provided no support. In the recent case of *In re Rouffet* , 47 USPQ2d 1453, 1458 (Fed. Cir. 1998), the Court held that

> "the examiner **must** show reasons that the skilled artisan, **confronted with the same problems** as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed." (emphasis added)

Nowhere in either of the cited references does there appear to be any recognition of the problem solved by the claimed invention.

(a) Only the Kizuki reference relates to a single electron transistor (SET)

The Examiner correctly notes that Kizuki discloses a conventional prior art single electron transistor. However, the Examiner appears to ignore the fact that

both Chapple-Sokol and Doyle relate only to field effect transistors (FETs). The FETs use quantum wire channels for high electron mobility in order to provide a higher speed of operation for the field effect transistors. The Examiner admits that "Bestwick does not explicitly disclose the use of a quantum wire in a transistor structure." In fact, Bestwick has no disclosure of the use of a quantum wire with any other electronic structures, i.e. source, drain or gate electrodes, all of which are necessary to form any type of transistor, let alone in an arrangement which forms a SET.

Thus, only Kizuki is pertinent to appellants' independent claim 1 which by definition recites the structure and structural interrelationship which results in an SET. For example, claim 1 recites that the first semiconductor comprises the substantially one-dimensional elongate conducting means and that it is substantially surrounded by a second semiconductor. The claim requires that this first semiconductor extend between source and drain electrodes, and there is a further electrode noted in the region of the first semiconductor and that electrode operates in the manner of a gate electrode. The first semiconductor forming the one-dimensional elongate conductor is provided in a groove between the two layers of the second semiconductor (layers 12 and 13 in Figure 2).

Thus, the location of the first semiconductor within the second semiconductor serves as hard containment and in combination with the other

elements ensures SET operation. The citations to references other than Kizuki are unrelated to SET technology and/or problems with SET technology.

(b) Kizuki teaches away from the claimed combination of elements;

The Kizuki reference, the only reference relating to an SET-type device, specifically teaches away from appellants' claimed invention. The Kizuki device utilizes quantum wires which are formed by soft confinement, i.e. an electrical field which is applied by the saw-tooth structure labeled 3 and 4 in Figure 1.

There is no disclosure in Kizuki of a first semiconductor (which forms the substantially one-dimensional elongate conductor) which is "substantially surrounded by a second semiconductor." If item 7 shown in Kizuki's Figure 1 and labeled the "electron storage regions" are in fact quantum wires, there is no teaching that they are surrounded by a second semiconductor and that they are provided in a groove. Rather, at best, they are located in layer 2 and have grooved structures 3 and 4 located above them. Thus, the Kizuki device is simply a different structure for an SET device and therefore would lead one of ordinary skill in the art away from appellants' claimed combination of elements.

As noted above in the case of *In re Fine* and elsewhere, there can be no obviousness when the single pertinent reference, i.e. Kizuki, teaches away from appellants' claimed combination of elements.

(c) No cited reference suggests the problem solved by the present invention, i.e. SET operation at higher temperatures

As noted above and in appellants' specification, the problem solved by the present invention is the ability to have higher temperature SET devices. While the prior art devices had to be located in an extremely cold environment, the present invention avoids this necessity by its combination of elements. None of the cited prior art references appear to be even aware of this problem, let alone attempt to provide a solution to the problem. Quite clearly, Chapple-Sokol and Doyle relate to FETs and thus don't address problems with SETs. Bestwick doesn't even relate to transistors at all. Kizuki relates to conventional SET devices and does not appear to be aware of the problem, let alone the fact that there could be a potential solution to the problem.

As noted above, in *In re Rouffet*, where none of the prior art references indicate any awareness of or even address the problem solved by the present invention, there can be no case for obviousness.

(d) The Examiner fails to provide any reason or motivation for combining any of the prior art references

The Examiner's conclusory statement that "it would be obvious to use the quantum wire of Bestwick as the channel of Kizuki so as to attain a device with high electron mobility" as presumably taught by Chapple-Sokol and/or Doyle is not the required "suggestion" or "motivation" for combining references required by

the Court of Appeals for the Federal Circuit in order to establish a *prima facie* case of obviousness.

In the present case, the Examiner requires elements taken from four separate references, only one of which even remotely resembles the subject matter of the claimed invention. The Examiner has pointed to no reason or motivation why one would combine anything from Bestwick which discloses only the use of a quantum wire (which the Examiner admits is not with respect to a transistor).

There is no reason why one would take elements from the field effect transistors of Chapple-Sokol and Doyle and attempt to use them in a SET device. Since only the Kizuki reference relates to an SET and it teaches away from the claimed combination, there is no basis for claiming that it would be obvious to combine the elements. Moreover, since Chapple-Sokol and Doyle teach an FET and not an SET, any teachings in those references would not normally be combined to form an SET, even if Kizuki did not teach away from the claimed combination.

None of the references, including Kizuki, teach the problem of higher temperature operation. In accordance with the standard set out by the Court of Appeals for the Federal Circuit in *In re Rouffet*, none of the art cited even recognizes the problem solved by the claimed invention. Accordingly, the Office has simply failed to meet the burden of establishing a *prima facie* case of

obviousness, because it has failed to provide any reason or motivation for combining four separate prior art references.

IX. CONCLUSION

The Examiner has failed to establish a *prima facie* case of obviousness by apparently failing to appreciate that only one of the four references relates to an SET and that reference teaches away from the combination of elements recited in appellants' claims. The subsidiary references teach structural relationships, but in settings unrelated to SETs (two are related to FETs and the third only teaches a quantum wire, which the Examiner admits is unrelated to a transistor structure). Nowhere in the cited prior art does the Examiner indicate how or where there is any recognition of the problem solved by the present invention, and accordingly there is clearly no reason or motivation for combining this prior art.

Because of the above reasons, the Patent Office has failed to establish a *prima facie* case of obviousness under the provisions of 35 USC §103, or if established, appellants have completely and properly rebutted any such case made and has clearly established the novelty and non-obviousness of the claimed invention. In view of the above, the rejection of claims 1-7, 9, 10, 12-21, 23-26, 29, 30 and 32 is clearly in error and reversal thereof by this Honorable Board is respectfully requested.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____

Stanley C. Spooner
Reg. No. 27,393

SCS:kmm
Enclosures
Appendix A - Claims on Appeal

APPENDIX A

Claims on Appeal

1. A transistor comprising at least one, substantially one-dimensional, elongate conducting means provided by at least a first semiconductor substantially surrounded by a second semiconductor and extending between source and drain electrodes, and in which there is provided at least one further electrode in a region of the at least one elongate conducting means, the at least one elongate conducting means being provided in a groove within the second semiconductor, said groove being oriented such that at least one wall of the groove is a, substantially planar, surface, substantially parallel to a crystal plane on which the growth rate of the first semiconductor is substantially zero.

2. A transistor according to claim 1 wherein the groove is provided by an intersection of two walls, each wall being a substantially planar, surface, roughly parallel to a crystal plane on which the growth rate of the first semiconductor is substantially zero.

3. A transistor according to claim 2 wherein the first semiconductor is provided in a region of the intersection.

4. A transistor according to claim 1 comprising a groove formed into a substrate having a region of the second semiconductor provided on the sides of the grooves lining the groove.

5. A transistor according to claim 4 wherein the first semiconductor and the substrate are substantially the same material.

6. A transistor according to claim 1 wherein the conducting means comprises an elongate region of the first semiconductor in a bottom region of the second semiconductor, that is in a bottom region of the lined groove.

7. A transistor according to claim 1 wherein the groove is provided within a top region of a mesa structure.

8. A transistor according to claim 1 wherein said at least one elongate conducting means comprises two elongate conducting means.

9. A transistor according to claim 1 wherein a quantum dot is provided along a region of the conducting means.

10. A transistor according to claim 9 wherein the at least one further electrode is adapted, in use, to provide the confinement to provide the quantum dot.

11. A transistor according to claim 9 wherein there are provided a plurality of quantum dots along the conducting means.

12. A transistor according to claim 1 wherein said at least one further electrode is arranged to provide confinement in a third dimension for charge carriers within the conducting means, in which hard confinement in two dimensions holds charge carriers within the conducting means.

13. A transistor according to claim 1 wherein said at least one further electrode is arranged substantially transverse to the conducting means.

14. A transistor according to claim 1 wherein said at least one further electrode is arranged to cause a peak within the energy bands of the first semiconductor of the conducting means.

15. A transistor according to claim 1 wherein a portion of the conducting means has a crescent shaped cross section.

16. A transistor according to claim 1 wherein the first semiconductor is gallium arsenide (GaAs).

17. A transistor according to claim 1 wherein the second semiconductor is aluminium gallium arsenide (AlGaAs).

18. A transistor according to claim 1 which is a single electron transistor.

19. A method of providing the transistor according to claim 1 comprising:

providing a substantially one-dimensional elongate conducting means by providing a first semiconductor substantially surrounded by a second semiconductor material, the elongate conducting means being provided by creating a groove of second semiconductor such that at least one wall of the groove is a substantially planer surface roughly parallel to a crystal plane on which the growth rate of the first semiconductor is substantially zero and subsequently providing the first semiconductor in the groove,

providing a source electrode at a first end region of the conducting means and a drain electrode at a second end region of the conducting means, and providing at least one further gate electrode in a region of the conducting means.

20. A method according to claim 19 comprising providing the groove by performing an anisotropic etch.

21. A method according to claim 19 wherein the groove is provided in an n^+ epilayer grown onto a substrate.

22. A method according to claim 21 wherein the substrate and first semiconductor are substantially the same material.

23. A method according to claim 21 wherein the groove is provided in a p^- doped region provided in a top region of the n^+ epilayer.

24. A method according to claim 19 wherein the groove of second semiconductor is provided by lining a groove with second semiconductor.

25. A method according to claim 24 wherein the first semiconductor is grown in a bottom region of the lined groove.

26. A method according to claim 19 wherein the first semiconductor is surrounded by the second semiconductor by provision of a layer of second semiconductor once the first semiconductor has been provided.

27. A method according to claim 19 wherein the first material is GaAs.

28. A method according to claim 19 wherein the second semiconductor is AlGaAs.

29. A method according to claim 19 wherein the groove is arranged such that the walls of the groove lies substantially along the (111) planes of the semiconductor.

30. A method according to claim 19 wherein the groove in the substrate is formed slightly off axis from the planes of the semiconductor.

31. A method according to claim 30 wherein quantum dots are provided along the conducting means in the vicinity of stops caused due to thickness variations of the conducting means due to the off axis groove.

32. A method according to claim 19 wherein the transistor is a single electron transistor (SET).